



501.390555CX1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: N. HASEGAWA, et al.  
Serial No.: 10/674,381  
Filed: October 1, 2003  
Title: METHOD OF MANUFACTURING SEMICONDUCTOR  
INTEGRATED CIRCUIT DEVICE OPTICAL MASK THEREOF,  
ITS MANUFACTURING METHOD, AND MASK BLANKS  
Group: 1756

**REQUEST FOR CORRECTED FILING RECEIPT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

February 10, 2003

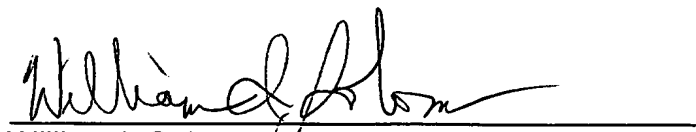
Sir:

Attached hereto is the Official Filing Receipt for the above-identified application, wherein it is noted that the Domestic Priority data is incorrect.

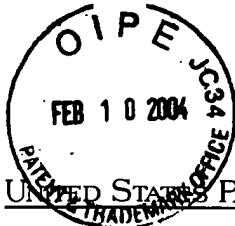
Accordingly, it is respectfully requested that a corrected filing receipt be issued indicating that the Domestic Priority data to be – **CON of 09/646,036 09/13/2000 (now U.S. Patent 6,677,107 01/13/2004)** – instead Con of 09/464,036 12/15/1999 ABN.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

  
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Registration No.: 28,565

WIS/rr  
Attachments



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/674,381	10/01/2003	1756	1506	501.39055CX1	17	37	8

CONFIRMATION NO. 4390

020457  
ANTONELLI, TERRY, STOUT & KRAUS, LLP  
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ARLINGTON, VA 22209-9889

## FILING RECEIPT



\*OC000000011555479\*

Date Mailed: 12/23/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

## Applicant(s)

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Tsuneo Terasawa, Ome, JAPAN;  
Toshihiko Tanaka, Tokyo, JAPAN;

## Domestic Priority data as claimed by applicant

This application is a CON of 09/464,036 12/15/1999 ABN -- con of 09/646,036 09/13/2000

## Foreign Applications

JAPAN 11-185221 06/30/1999

(Now US Patent 6,677,107  
01/13/2004)

If Required, Foreign Filing License Granted: 12/20/2003

Projected Publication Date: 04/01/2004

Non-Publication Request: No

Early Publication Request: No

## Title

Method of manufacturing semiconductor integrated circuit device optical mask therefor, its

manufacturing method, and mask blanks

**Preliminary Class**

430

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Title 37, Code of Federal Regulations, 5.11 & 5.15**

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